## Lesson Plan

Discipline		: Computer Science and Engineering				
Semester		: 3 <sup>rd</sup> (odd), (CSE 210L)				
Subject Duration		<ul> <li>Computer architecture and organization</li> <li>15 weeks (from Aug to Dec -2023)</li> </ul>				
Week		Theory		Topic Covered Date and Remarks		
Week	Lecture Day	Topic (Including Assignment/Test)	Date	HOD	Director-Principa	
1 st	1.	Basic Boolean algebra and logic gates				
	2.	Combinational logic blocks				
	3.	Adder subtractor and multiplexers				
2 <sup>nd</sup>	4	Sequential logic blocks				
	5	Flip flops,register,counter				
	6	Flynn's classification				
3 <sup>rd</sup>	7	Multilevel viewpoint of a machine				
	8	Digital logic				
	9	Micro architectures				
4 <sup>th</sup>	10	Operating systems				
	11	Performance matrix				
	12	Cpu architecture types				
5 <sup>th</sup>	13	Computer registers, stack memory				
	14	Detailed data path of a typical cpu				
	15	Computer organization concept				
<b>c</b> .1	16	Stored program concept				
6 <sup>th</sup>	17	Instruction codes, Instruction cycles				
	18	Timing and control, Types of instructions				
7 <sup>th</sup>		1 <sup>st</sup> Minor Test				
8 <sup>th</sup>	19	Memory reference, register reference				
	20	I/o reference instructions				
	21	Accumulator logic				
9 <sup>th</sup>	22	Control memory				
	23	Introduction to parallelism				
	24	Goals of parallelism and Amdahl's law				
10 <sup>th</sup>	25	Instruction level parallelism				
	26	Processor level parallelism				
	27	Pipelining and its features				
11 <sup>th</sup>	28	Super scaling overview				
	29	Multiprocessor systems overview				
	30	Memory hierarchy				
12 <sup>th</sup>	31	I/O techniques				
	32	Need of memory and examples				
	33	Cache memory and main memory				
13 <sup>th</sup> -	34	Stack organization, Instruction formats				
	35	Addressing modes, Types of various modes				
	36	Address sequencing, Instruction set architectures				
14 <sup>th</sup>		2 <sup>nd</sup> Minor Test				
15 <sup>th</sup>	37	Micro instructions, Classification of processors				
	38	Micro program sequencer, Ram and Rom organization				
	39	Implementation of control unit, DMA modes of transfer				