

## Lesson Plan

**Name of Faculty** : Dr. Suman Rani, Guest Faculty of ECE  
**Discipline** : Electronics & communication Engg.  
**Semester** : 5<sup>th</sup> (odd)  
**Subject** : Computer architecture and organization (PC/ECE/54-T)

Week	Theory		Topic Covered Date and Remarks		
	Lecture Day	Topic (Including Assignment/Test)	Date	HOD	Director-Principal
1 <sup>st</sup>	1	<b>INTRODUCTION</b> Boolean algebra and Logic gates			
	2	Adders, Subtractors			
	3	Multiplexers, Encoders			
2 <sup>nd</sup>	4	Decoders, Demultiplexers			
	5	Flip-Flops, Registers			
	6	K-map, counters			
3 <sup>rd</sup>	7	<b>REGISTER TRANSFER &amp; MICRO OPERATIONS</b> Register transfer language, register transfer			
	8	bus and memory transfer			
	9	Arithmetic, Logic and Shift microoperations			
4 <sup>th</sup>	10	Arithmetic logic shift unit			
	11	<b>COMPUTER ORGANIZATION AND DESIGN.</b> Store program control concept			
	12	computer registers and instruction			
5 <sup>th</sup>	13	timing and control, instruction cycle,			
	14	memory reference instruction, input-output and interrupt			
	15	design of basic computer and accumulator logic			
6 <sup>th</sup>	16	<b>MICRO PROGRAMMED CONTROL</b> Control memory, address sequencing			
	17	microinstruction formats, micro-program sequencer			
	18	Implementation and design of control unit.			
7 <sup>th</sup>	19	<b>CPU &amp; PARALLEL PROCESSING</b> Introduction of central processing unit			
	20	general register organization			
	21	stack organization			
8 <sup>th</sup>	22	instruction format			
	23	addressing mode and its type			
	24	operations in the instruction set			
9 <sup>th</sup>	25	Instruction set based classification of processors			
	26	parallel processing			
	27	introduction of Pipelining and its type			
10 <sup>th</sup>	28	vector and array processing.			
	29	<b>MEMORY HIERARCHY &amp; I/O TECHNIQUES</b> The need for a memory hierarchy			
	30	Type of Memory: Main memory			
11 <sup>th</sup>	31	Static and dynamic memory			
	32	Auxiliary memory			
	33	Casche memory			
12 <sup>th</sup>	34	Virtual memory			
	35	Associate memory			
	36	Memory management			
13 <sup>th</sup>	37	Input output interface			
	38	mode of transfer			
	39	MCQ based on Unit 1& 2			