**Lesson Plan**

Name of faculty : Mr. Surender

Discipline : Electrical Engineering

Semester : 4th

Subject : Digital Electronics (EE-206L)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Week | Theory | | **Date of Actual covered** | **Signatures** | | | | | |
| Lecture  Day | Topic (Including assignment / Test) | **Concerned teacher** | | | **HOD** | **DP** | |
| **Unit-I** | | | | | | | | | |
| 1st | 1 | **FUNDAMENTALS OF DIGITAL TECHNIQUES** |  | |  |  | | |  |
| 2 | Introduction to Signal and its types |
| 3 | Analog nad Digital Signal |
| 4 | Introduction to logic gates |
| 2nd | 5 | AND, OR, NOT |  | |  |  | | |  |
| 6 | NAND, NOR, EX-OR |
| 7 | EX-NOR, and their applications |
| 8 | Related Problem Analysis |
| 3rd | 9 | Boolean algebra and Numerical problems |  | |  |  | | |  |
| 10 | Review of Number systems. |
| 11 | Binary codes: BCD, Excess-3, Gray, EBCDIC |
| 12 | ASCII, Error detection and correction codes. |
| **Unit-II** | | | | | | | | | |
| 4th | 13 | **COMBINATIONAL DESIGN USING GATES** |  | |  |  | | |  |
| 14 | Design using gates, Karnaugh map |
| 15 | Numerical Problems |
| 16 | Quine Mcluskey methods of simplification |
| 5th | 17 | Numerical Problems |  | |  |  | | |  |
| 18 | **COMBINATIONAL DESIGN USING MSI DEVICES** |
| 19 | Multiplexers and Demultiplexers |
| 20 | And their use as logic elements |
| 6th | 21 | Decoders, Adders / Subtractors |  | |  |  | | |  |
| 22 | BCD arithmetic circuits |
| 23 | Encoders, Decoders |
| 24 | Drivers for display devices |
| **7th** | **1st Minor Test** | | | | | | | | |
| **Unit-III** | | | | | | | | | |
| 8th | 25 | **SEQUENTIAL CIRCUITS:** Flip-Flops |  | |  |  | | |  |
| 26 | S-R, J-K, T, D, master-slave, edge triggered |
| 27 | Shift registers, sequence generators, Counters |
| 28 | Asynchronous and Synchronous Counters. |
| 9th | 29 | Ring counters and Johnson Counter |  | |  |  | | |  |
| 30 | Design of Synchronous Asynchronous circuits |
| 31 | **A/D AND D/A CONVERTERS** Sample and hold ckt. |
| 32 | Weighted resistor and R -2 R ladder D/A Converters |
| 10th | 33 | Specifications for D/A converters. A/D converters |  | |  |  | | |  |
| 34 | Quantization, parallel –comparator |
| 35 | Successive approximation, counting type. |
| 36 | Dual-slope ADC, specifications of ADCs. |
| **Unit-IV** | | | | | | | | | |
| 11th | 37 | **DIGITAL LOGIC FAMILIES** |  | |  |  | | |  |
| 38 | Switching mode operation of p-n junction |
| 39 | Bipolar and MOS. Devices |
| 40 | Bipolar logic families |
| 12th | 41 | Introduction to RTL, DTL |  | |  |  | | |  |
| 42 | Introduction to DCTL, HTL |
| 43 | Introduction to TTL, ECL |
| 44 | MOS, and CMOS logic families |
| 13th | 45 | Introduction Tristate logic, |  | |  |  | | |  |
| 46 | Interfacing of CMOS and TTL Faimily |
| 47 | **PROGRAMMABLE LOGIC DEVICES** |
| 48 | Introduction to RAM, ROM. |
| **14th** | **2nd Minor test** | | | | | | | | |
| 15th | 49 | Differentiate between RAM and ROM |  | |  |  | | |  |
|  | 50 | Introduction to PLA, PAL |
|  | 51 | Introduction to FPGA and CPLDs |
|  | 52 | Related Problem Discussion. |

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Subject : Digital Electronics Lab (EE-206P)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Week** | **Practical** | | | | **Date of Actual covered** | **Signature** | | |
|  |  |  | **Practical**  **Day** | **Topic** | **Concerned teacher** | **HOD** | **DP** |
| 1st | 1 |  | 1 | Study of TTL gates – AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR |  |  |  |  |
| 2 |  |
| 3 |  |
| 4 |  |
| 2nd | 5 |  | 2 | Design & realize a given function using K-maps and verify its performance |  |  |  |  |
| 6 |  |
| 7 |  |
| 8 |  |
| 3rd | 9 |  | 3 | To verify the operation of multiplexer & Demultiplexer. |  |  |  |  |
| 10 |  |
| 11 |  |
| 12 |  |
| 4th | 13 |  | 4 | To verify the operation of comparator |  |  |  |  |
| 14 |  |
| 15 |  |
| 16 |  |
| 5th | 17 |  | 5 | To verify the truth tables of S-R, J-K, T & D type flip flops. |  |  |  |  |
| 18 |  |
| 19 |  |
| 20 |  |
| 6th | 21 |  | 6 | To verify the operation of bi-directional shift register |  |  |  |  |
| 22 |  |
| 23 |  |
| 24 |  |
| **7th** | **1st Minor Test** | | | |  |  |  |  |
| 8th | 25 |  | 7 | Viva-Voice 1st |  |  |  |  |
| 26 |  |
| 27 |  |
| 28 |  |
| 9th | 29 |  | 8 | To design & verify the operation of 3-bit synchronous counter. |  |  |  |  |
| 30 |  |
| 31 |  |
| 32 |  |
| 10th | 33 |  | 9 | To design and verify the operation of synchronous UP/DOWN decade counter using J K flip-flops & drive a seven-segment display using the same |  |  |  |  |
| 34 |  |
| 35 |  |
| 36 |  |
| 11th | 37 |  | 10 | To design and verify the operation of asynchronous UP/DOWN decade counter using J K flip-flops & drive a seven-segment display using the same. |  |  |  |  |
| 38 |  |
| 39 |  |
| 40 |  |
| 12th | 41 |  | 11 | To design & realize a sequence generator for a given sequence using J-K flip-flops. |  |  |  |  |
| 42 |  |
| 43 |  |
| 44 |  |
| 13th | 45 |  | 12 | Design a 4-bit shift-register and verify its operation . Verify the operation of a ring counter and a Johnson counter. |  |  |  |  |
| 46 |  |
| 47 |  |
| 48 |  |
| **14th** | **2nd Minor test** | | | |  |  |  |  |
| 15th | 49 |  | 13 | Viva-Voice – 2nd |  |  |  |  |
|  | 50 |  |
|  | 51 |  |
|  | 52 |  |