Lesson Plan

Name of Faculty : **Ms. Varsha Rani, Assistant Professor of CSE**
Discipline : **Computer Science and Engineering**
Semester : **7TH (ODD)**
Subject : **Advance Computer Architecture (CSE-401 E)**
Lesson Plan Duration : **15 weeks (from July/August-2020 to Nov/Dec-2020)**
Work Load (Lecture/Practical) per week (in hours): Lectures-04 hours

Week	Theory		Topic Covered Date and Remarks		
	Lecture- Day	Topic (Including Assignment/Test)	Date	HOD	Director- Principal
1st	1	The State Of Computing			
	2	Multiprocessor			
	3	Multi Computers			
	4	Multi Vectors			
2nd	5	SIMD Computers			
	6	PRAM model			
	7	VLSI model			
	8	Problem on 1st unit			
3rd	9	Condition on Parallelism			
	10	Program Partitioning			
	11	Program SCHEDULING			
	12	Program Flow Mechanism			
4th	13	System Interconnect Architecture			
	14	Numerical on Scheduling			
	15	Component Used On interconnection			
	16	Problem on 2nd unit			
5th	17	Advance Processor Technology			
	18	Super Scalar Processor			
	19	Vector Processor			
	20	Memory Hierarchy Technology			
6th	21	Numerical on Memory			
	22	Numerical on processor			
	23	Virtual memory technology			
	24	Problems on 3rd unit			
7th		**1st Minor Test**			
8th	25	Backplane Bus system			
	26	Cache Memory Organisation			
	27	Shared Memory Organisation			
	28	Sequential Consistency Model			
9th	29	Numerical related to sequential model			
	30	Week Consistency Model			
	31	Numerical related to Model			
	32	Problem on 4th unit			
10th	33	Linear Pipeline Processor			
	34	Non linear Pipeline Processor			
	35	Instruction Pipeline Design			
	36	Arithmetic Pipeline design			
11th	37	Superscalar Design			
	38	Super Pipeline Design			
	39	Multiprocessor System Interconnect			
	40	Cache Coherence			
12th	41	Synchronization Mechanism			
	42	Message Passing Mechanism			
	43	Problem on 5th unit			
	44	Problem on 6TH unit			
13th	45	Vector Processing Principle			
	46	Multi vector Processor			
	47	Compound Vector Processing			
	48	Principle of Multi threading			
14th		**2nd Minor Test**			
15th	49	Data Flow Architecture			
	50	Hybrid Architecture			
	51	Numerical on Vector Processor			
	52	Problem Solution			

Sr.	Comments	HOD	Director- Principal
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