Lesson Plan

**Lesson Plan**

**Name of Faculty :**  Poonam

**Discipline :** BTech CSE

**Semester :** 5th

**Subject :** Principles of Digital Electronics (OE-ECE-391-T)

**Lesson Plan Duration:** 15 weeks

Work Load (Lecture/Practical) per week (in hours): **Lectures 03 hours**.

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| **Week** | **Lecture** | **Topic (Including Assignment / Test) : Planned** | **Actually covered on**  **(date)** | **Teacher’s**  **Sign** |
| 1st | 1 | Decimal,Binary,octal ,hexadecimal |  |  |
| 2 | 1’s ans 2’s complements |  |  |
| 3 | Binary codes: BCD, Excess-3, Gray |  |  |
| 2nd | 4 | Alphanumeric codes,Boolean theorems |  |  |
| 5 | Universal gates |  |  |
| 6 | Sum of products,product of sums,MIN TERMS,MAX TERMS |  |  |
| 3rd | 7 | K-MAP |  |  |
| 8 | Quine-McCluskey method of minimization |  |  |
| 9 | Design of half adder and full adder |  |  |
| 4th | 10 | Half and full subtractors |  |  |
| 11 | Binary parallel adder,carry look ahead adder |  |  |
| 12 | Bcd adder, |  |  |
| 5th | 13 | Multiplexer, |  |  |
| 14 | Demultiplexer |  |  |
| 15 | Magnitude comparator |  |  |
| 6th | 16 | Decoder |  |  |
| 17 | Encoder |  |  |
| 18 | Priority Encoder |  |  |
| **7th** |  | **1stSessionals** |  |  |
| 8th | 19 | SR,JK Flip Flop |  |  |
| 20 | T,D FF |  |  |
| 21 | Master Slave FF |  |  |
| 9th | 22 | Triggering of FF,Conversion of FF |  |  |
| 23 | Ripple counter |  |  |
| 24 | Ring counter |  |  |
| 10th | 25 | Shift Register,Universal Shift Register |  |  |
| 26 | ROM,PROM |  |  |
| 27 | EPROM,EEPROM |  |  |
| 11th | 28 | EAPROM |  |  |
| 29 | RAM,Static and Dynamic RAM |  |  |
| 30 | PLA |  |  |
| 12th | 31 | PAL |  |  |
| 32 | FPGA |  |  |
| 33 | Logic levels |  |  |
| 13th | 34 | Propagation delay |  |  |
| 35 | Power Dissipation |  |  |
| 36 | Fan in,Fan out |  |  |
| **14th** |  | **2ndSessionals** |  |  |
| 15th | 37 | Noise Margin |  |  |
| 38 | RTL,TTL |  |  |
| 39 | ECL,CMOS |  |  |