Lesson Plan

Name of Faculty : Ms. Varsha, AP (CSE)

Discipline : Computer Science and Engineering Semester : 7th (odd), (CSE 210L)

Subject : Computer architecture and organization

Duration : 15 weeks (from Aug to Dec -2022)

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| **Week** | **Theory** | | **Topic Covered Date and Remarks** | | |
| **Lecture Day** | **Topic (Including Assignment/Test)** | **Date** | **HOD** | **Director-Principal** |
| 1st | 1. | Basic Boolean algebra and logic gates |  |  |  |
| 2. | Combinational logic blocks |  |  |  |
| 3. | Adder subtractor and multiplexers |  |  |  |
| 2nd | 4 | Sequential logic blocks |  |  |  |
| 5 | Flip flops,register,counter |  |  |  |
| 6 | Flynn’s classification |  |  |  |
| 3rd | 7 | Multilevel viewpoint of a machine |  |  |  |
| 8 | Digital logic |  |  |  |
| 9 | Micro architectures |  |  |  |
| 4th | 10 | Operating systems |  |  |  |
| 11 | Performance matrix |  |  |  |
| 12 | Cpu architecture types |  |  |  |
| 5th | 13 | Computer registers, stack memory |  |  |  |
| 14 | Detailed data path of a typical cpu |  |  |  |
| 15 | Computer organization concept |  |  |  |
| 6th | 16 | Stored program concept |  |  |  |
| 17 | Instruction codes , Instruction cycles |  |  |  |
| 18 | Timing and control, Types of instructions |  |  |  |
| 7th |  | **1st Minor Test** | | |  |
| 8th | 19 | Memory reference ,register reference |  |  |  |
| 20 | I/o reference instructions |  |  |  |
| 21 | Accumulator logic |  |  |  |
| 9th | 22 | Control memory |  |  |  |
| 23 | Introduction to parallelism |  |  |  |
| 24 | Goals of parallelism and Amdahl’s law |  |  |  |
| 10th | 25 | Instruction level parallelism |  |  |  |
| 26 | Processor level parallelism |  |  |  |
| 27 | Pipelining and its features |  |  |  |
| 11th | 28 | Super scaling overview |  |  |  |
| 29 | Multiprocessor systems overview |  |  |  |
| 30 | Memory hierarchy |  |  |  |
| 12th | 31 | I/O techniques |  |  |  |
| 32 | Need of memory and examples |  |  |  |
| 33 | Cache memory and main memory |  |  |  |
| 13th | 34 | Stack organization, Instruction formats |  |  |  |
| 35 | Addressing modes, Types of various modes |  |  |  |
| 36 | Address sequencing, Instruction set architectures |  |  |  |
| 14th |  | **2nd Minor Test** | | |  |
| 15th | 37 | Micro instructions, Classification of processors |  |  |  |
| 38 | Micro program sequencer, Ram and Rom organization |  |  |  |
| 39 | Implementation of control unit, DMA modes of transfer |  |  |  |